Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An architecture for a pipeline processor, comprising-:

a plurality of stages-;

a forwarding network of forwarding paths which connect said stages; and

a register file for operand write-back, wherein one of said stages includes an optimization-of-power-consumption function via inhibition of writing and subsequent readings in said register file of operands retrievable from said forwarding network because of reduced liveness lengths of said operands, wherein said function is configured for performing selectively, for a register of said register file assigned by a first instruction comprising a write-back stage and used by a second instruction, the following:

disabling of write-back of said register in said register file in the write-back stage of said first instruction; and

inhibiting assertion of a read address of said register in said register file by said second instruction.

2. (Canceled)

3. (Original) An architecture according to claim 1 wherein said one of said stages includes dedicated logic for disabling the write-enable signals that enable writing in said register file.

4. (Original) An architecture according to claim 3 wherein the one of said stages is a decoding stage for decoding the instructions and reading the operands from said register file, and said dedicated logic is included in said decoding stage.

5. (Original) An architecture according to claim 1, further comprising dedicated logic which minimizes read-port switching activity in said register file by maintaining values on the input read addresses of the register file at previous clock cycles.

6. (Original) An architecture according to claim 1 wherein said processor is a superscalar processor comprising a hardware control unit capable of analyzing an instruction window to determine liveness lengths of registers of the register file.

7. (Original) An architecture according to claim 1 wherein said architecture is configured as a VLIW architecture, in which a decision of activating said function is delegated to a compiler.

8. (Original) An architecture according to claim 7 wherein the compiler transfers information to hardware control logic, reserving specific operation bits in instruction encoding.

9. (Original) An architecture according to claim 7 wherein the compiler transfers information to hardware control logic, exploiting unused instruction encoding bits.

10. (Original) An architecture according to claim 1, further comprising interstage registers comprised between the stages for storing a volatile architectural state, and wherein the architecture is configured for discarding elements that exit said volatile architectural state, avoiding write-back in said register file.

11. (Currently Amended) An architecture according to claim 10 wherein the architecture is adapted to operate on instructions configurable as exceptions, and-, in order to ensure re-execution of instructions constituting an exception in a correct processor state, to write-back ~~is envisaged of~~ values inhibited as regards writing in said register file in the presence of a signal that is configured as an exception.

12. (Currently Amended) An architecture according to claim 11 wherein the plurality of stages includes ~~it comprises~~ a decoding stage for decoding instructions and reading operands from said register file, an instruction-execution stage, and a memory-access stage, and said write-back ~~is envisaged~~occurs whenever an exception signal is generated in one of said stages.

13. (Currently Amended) An architecture according to claim 11 wherein, in the presence of an instruction configured as an exception, the architecture is configured for executing the instructions in the pipeline until their completion, ~~there being envisaged write-back, in said register file, of~~ the results of all the instructions in the pipeline being written back in said register file.

14. (Original) An architecture according to claim 1, further comprising interstage registers coupled between stages of the plurality of stages, including latch registers used as a memory layer for storing the operands.

15. (Original) An architecture according to claim 14 wherein said interstage registers are configured in such a way that they are visible to the compiler and are not visible to the programmer.

16. (Original) An architecture according to claim 14 wherein said interstage registers are not write-addressable, in so far as they are implicitly addressed.

17. (Original) An architecture according to claim 14 wherein said interstage registers are configured as a transient memory which cannot be associated to a machine state that can be saved in the event of an exception.

18. (Original) An architecture according to claim 17 wherein said architecture is configured in such a way that sequences of instructions that use said interstage registers are treated as atomic sequences that are not subject to interrupts.

19. (Currently Amended) An architecture according to claim 18 wherein ~~disabling of~~ any interrupt is ~~envisaged~~ disabled prior to start of said sequences, and a machine state is rendered stable prior to interrupt re-enabling by means of write-back in the register file or in the memory.

20. (Original) An architecture according to claim 17, further comprising a function of generation of two pseudo-instructions, one for checkpoint declaration and one for checkpoint release, with the provision of a shadow register, wherein a program counter is saved from an instant of checkpoint declaration, a machine state not being modifiable until checkpoint release, whereby, upon checkpoint release, the shadow register is reset and the interrupts are disabled atomically.

21. (Original) An architecture according to claim 20 wherein results computed between said two pseudo-instructions are entrusted to a real state of the processor with subsequent interrupt re-enabling to enable re-start of normal execution.

22. (Original) An architecture according to claim 20 wherein, in the presence of interrupts between said pseudo-instructions, the execution is made to restart, after handling of the interrupts, starting from the program counter stored in the shadow register.

23. (Original) An architecture according to claim 20 wherein all register writings comprised between said pseudo-instructions involve only said interstage registers, whereby said register file is involved only for data reading.

24. (Original) An architecture according to claim 20 wherein the register file includes a subset reserved for transient variables that are generated between said two pseudo-instructions and a liveness length of which exceeds a maximum value allowed by the pipeline.

25. (Original) An architecture according to claim 24 wherein the first appearance of transient registers in a sequence being checkpointed is a definition such as a load

or write in a register, which can be seen as a constituent part of the machine state after checkpoint release.

26. (Canceled)

27. (New) An architecture for a pipeline processor, comprising:

a plurality of stages;

a forwarding network of forwarding paths which connect said stages; and

a register file for operand write-back, wherein one of said stages includes an optimization-of-power-consumption function via inhibition of writing and subsequent readings in said register file of operands retrievable from said forwarding network because of reduced liveness lengths of said operands, wherein said one of said stages includes dedicated logic for disabling the write-enable signals that enable writing in said register file, wherein the one of said stages is a decoding stage for decoding the instructions and reading the operands from said register file, and said dedicated logic is included in said decoding stage.

28. (New) An architecture according to claim 27, further comprising dedicated logic which minimizes read-port switching activity in said register file by maintaining values on the input read addresses of the register file at previous clock cycles.

29. (New) An architecture according to claim 27 wherein said processor is a superscalar processor comprising a hardware control unit capable of analyzing an instruction window to determine liveness lengths of registers of the register file.

30. (New) An architecture according to claim 27 wherein said architecture is configured as a VLIW architecture, in which a decision of activating said function is delegated to a compiler.

31. (New) An architecture according to claim 30 wherein the compiler transfers information to hardware control logic, reserving specific operation bits in instruction encoding.

32. (New) An architecture according to claim 30 wherein the compiler transfers information to hardware control logic, exploiting unused instruction encoding bits.

33. (New) An architecture according to claim 27, further comprising interstage registers comprised between the stages for storing a volatile architectural state, and wherein the architecture is configured for discarding elements that exit said volatile architectural state, avoiding write-back in said register file.

34. (New) An architecture for a pipeline processor, comprising:

a plurality of stages;

a forwarding network of forwarding paths which connect said stages;

a register file for operand write-back, wherein one of said stages includes an optimization-of-power-consumption function via inhibition of writing and subsequent readings in said register file of operands retrievable from said forwarding network because of reduced liveness lengths of said operands; and

dedicated logic which minimizes read-port switching activity in said register file by maintaining values on the input read addresses of the register file at previous clock cycles.

35. (New) An architecture according to claim 34 wherein said processor is a superscalar processor comprising a hardware control unit capable of analyzing an instruction window to determine liveness lengths of registers of the register file.

36. (New) An architecture according to claim 34 wherein said architecture is configured as a VLIW architecture, in which a decision of activating said function is delegated to a compiler.

37. (New) An architecture according to claim 36 wherein the compiler transfers information to hardware control logic, reserving specific operation bits in instruction encoding.

38. (New) An architecture according to claim 36 wherein the compiler transfers information to hardware control logic, exploiting unused instruction encoding bits.

39. (New) An architecture according to claim 34, further comprising interstage registers comprised between the stages for storing a volatile architectural state, and wherein the architecture is configured for discarding elements that exit said volatile architectural state, avoiding write-back in said register file.

40. (New) An architecture for a pipeline processor, comprising:

a plurality of stages;

a forwarding network of forwarding paths which connect said stages;

a register file for operand write-back, wherein one of said stages includes an optimization-of-power-consumption function via inhibition of writing and subsequent readings in said register file of operands retrievable from said forwarding network because of reduced liveness lengths of said operands; and

interstage registers coupled between stages of the plurality of stages, including latch registers used as a memory layer for storing the operands, wherein said interstage registers are not write-addressable, in so far as they are implicitly addressed.

41. (New) An architecture according to claim 40, wherein said interstage registers store a volatile architectural state, and wherein the architecture is configured for discarding elements that exit said volatile architectural state, avoiding write-back in said register file.

42. (New) An architecture according to claim 41 wherein the architecture is adapted to operate on instructions configurable as exceptions, and, in order to ensure re-execution of instructions constituting an exception in a correct processor state, to write-back values inhibited as regards writing in said register file in the presence of a signal that is configured as an exception.

43. (New) An architecture according to claim 42 wherein the plurality of stages includes a decoding stage for decoding instructions and reading operands from said register file, an instruction-execution stage, and a memory-access stage, and said write-back occurs whenever an exception signal is generated in one of said stages.

44. (New) An architecture according to claim 42 wherein, in the presence of an instruction configured as an exception, the architecture is configured for executing the instructions in the pipeline until their completion, the results of all the instructions in the pipeline being written back in said register file.

45. (New) An architecture according to claim 40 wherein said interstage registers are configured as a transient memory which cannot be associated with a machine state that can be saved in the event of an exception.

46. (New) An architecture according to claim 45 wherein said architecture is configured in such a way that sequences of instructions that use said interstage registers are treated as atomic sequences that are not subject to interrupts.

47. (New) An architecture according to claim 46 wherein any interrupt is disabled prior to start of said sequences, and a machine state is rendered stable prior to interrupt re-enabling by means of write-back in the register file or in the memory.

48. (New) An architecture for a pipeline processor, comprising:

a plurality of stages;

a forwarding network of forwarding paths which connect said stages;

a register file for operand write-back, wherein one of said stages includes an optimization-of-power-consumption function via inhibition of writing and subsequent readings in said register file of operands retrievable from said forwarding network because of reduced liveness lengths of said operands; and

interstage registers coupled between stages of the plurality of stages, including latch registers used as a memory layer for storing the operands, wherein said interstage registers

are configured as a transient memory which cannot be associated to a machine state that can be saved in the event of an exception, wherein said architecture is configured in such a way that sequences of instructions that use said interstage registers are treated as atomic sequences that are not subject to interrupts.

49. (New) An architecture according to claim 48, wherein the interstage registers store a volatile architectural state, and wherein the architecture is configured for discarding elements that exit said volatile architectural state, avoiding write-back in said register file.

50. (New) An architecture according to claim 49 wherein the architecture is adapted to operate on instructions configurable as exceptions, and, in order to ensure re-execution of instructions constituting an exception in a correct processor state, to write-back values inhibited as regards writing in said register file in the presence of a signal that is configured as an exception.

51. (New) An architecture according to claim 50 wherein the plurality of stages includes a decoding stage for decoding instructions and reading operands from said register file, an instruction-execution stage, and a memory-access stage, and said write-back occurs whenever an exception signal is generated in one of said stages.

52. (New) An architecture according to claim 50 wherein, in the presence of an instruction configured as an exception, the architecture is configured for executing the instructions in the pipeline until their completion, the results of all the instructions in the pipeline being written back in said register file.

53. (New) An architecture according to claim 48 wherein said interstage registers are configured in such a way that they are visible to the compiler and are not visible to the programmer.

54. (New) An architecture according to claim 48 wherein any interrupt is disabled prior to start of said sequences, and a machine state is rendered stable prior to interrupt re-enabling by means of write-back in the register file or in the memory.

55. (New) An architecture for a pipeline processor, comprising:

a plurality of stages;

a forwarding network of forwarding paths which connect said stages;

a register file for operand write-back, wherein one of said stages includes an optimization-of-power-consumption function via inhibition of writing and subsequent readings in said register file of operands retrievable from said forwarding network because of reduced liveness lengths of said operands6. An architecture according to claim 1 wherein said processor is a superscalar processor comprising a hardware control unit capable of analyzing an instruction window to determine liveness lengths of registers of the register file;

interstage registers coupled between stages of the plurality of stages, including latch registers used as a memory layer for storing the operands, wherein said interstage registers are configured as a transient memory which cannot be associated to a machine state that can be saved in the event of an exception; and

a function of generation of two pseudo-instructions, one for checkpoint declaration and one for checkpoint release, with the provision of a shadow register, wherein a program counter is saved from an instant of checkpoint declaration, a machine state not being modifiable until checkpoint release, whereby, upon checkpoint release, the shadow register is reset and the interrupts are disabled atomically.

56. (New) An architecture according to claim 55 wherein results computed between said two pseudo-instructions are entrusted to a real state of the processor with subsequent interrupt re-enabling to enable re-start of normal execution.

57. (New) An architecture according to claim 55 wherein, in the presence of interrupts between said pseudo-instructions, the execution is made to restart, after handling of the interrupts, starting from the program counter stored in the shadow register.

58. (New) An architecture according to claim 55 wherein all register writings comprised between said pseudo-instructions involve only said interstage registers, whereby said register file is involved only for data reading.

59. (New) An architecture according to claim 55 wherein the register file includes a subset reserved for transient variables that are generated between said two pseudo-instructions and a liveness length of which exceeds a maximum value allowed by the pipeline.

60. (New) An architecture according to claim 59 wherein the first appearance of transient registers in a sequence being checkpointed is a definition such as a load or write in a register, which can be seen as a constituent part of the machine state after checkpoint release.